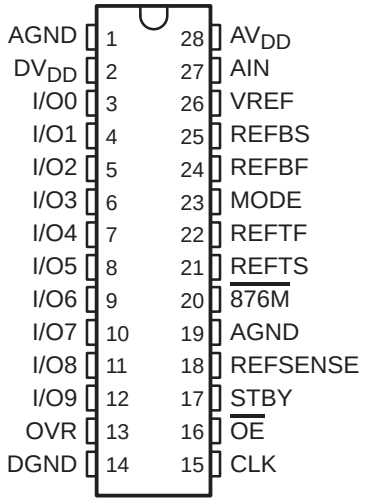
- **10-Bit Resolution, 30 MSPS Analog-to-Digital Converter**
- **Configurable Input: Single-Ended or Differential**
- **Differential Nonlinearity: ±0.3 LSB**
- **Signal-to-Noise: 57 dB**
- **Spurious Free Dynamic Range: 60 dB**
- **Adjustable Internal Voltage Reference**
- **Out-of-Range Indicator**
- **Power-Down Mode**
- **Pin Compatible With TLC876**

28-PIN TSSOP/SOIC PACKAGE (TOP VIEW)



description

The THS1030 is a CMOS, low-power, 10-bit, 30 MSPS analog-to-digital converter (ADC) that can operate with a supply range from 3 V to 5.5 V. The THS1030 has been designed to give circuit developers flexibility. The analog input to the THS1030 can be either single-ended or differential. The THS1030 provides a wide selection of voltage references to match the user's design requirements. For more design flexibility, the internal reference can be bypassed to use an external reference to suit the dc accuracy and temperature drift requirements of the application. The out-of-range output is used to monitor any out-of-range condition in THS1030's input range.

The speed, resolution, and single-supply operation of the THS1030 are suited for applications in STB, video, multimedia, imaging, high-speed acquisition, and communications. The speed and resolution ideally suit charge-couple device (CCD) input systems such as color scanners, digital copiers, digital cameras, and camcorders. A wide input voltage range between REFBS and REFTS allows the THS1030 to be applied in both imaging and communications systems.

The THS1030C is characterized for operation from 0°C to 70°C, while the THS1030I is characterized for operation from −40°C to 85°C

AVAILABLE OPTIONS

PRODUCT	PACKAGE LEAD	PACKAGE DESGIGNATOR†	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKINGS	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
THS1030C	TSSOP−28	PW	0°C to 70°C	TH1030	THS1030CPW	Tube, 50
					THS1030CPWR	Tube and Reel, 2000
THS1030I			−40°C to 85°C	TJ1030	THS1030IPW	Tube, 50
					THS1030IPWR	Tube and Reel, 2000
THS1030C	SOP−28	DW	0°C to 70°C	TH1030	THS1030CDW	Tube, 20
					THS1030CDWR	Tube and Reel, 1000
THS1030I			−40°C to 85°C	TJ1030	THS1030IDW	Tube, 20
					THS1030IDWR	Tube and Reel, 1000

† For the most current specification and package information, refer to the TI web site at *www.ti.com*.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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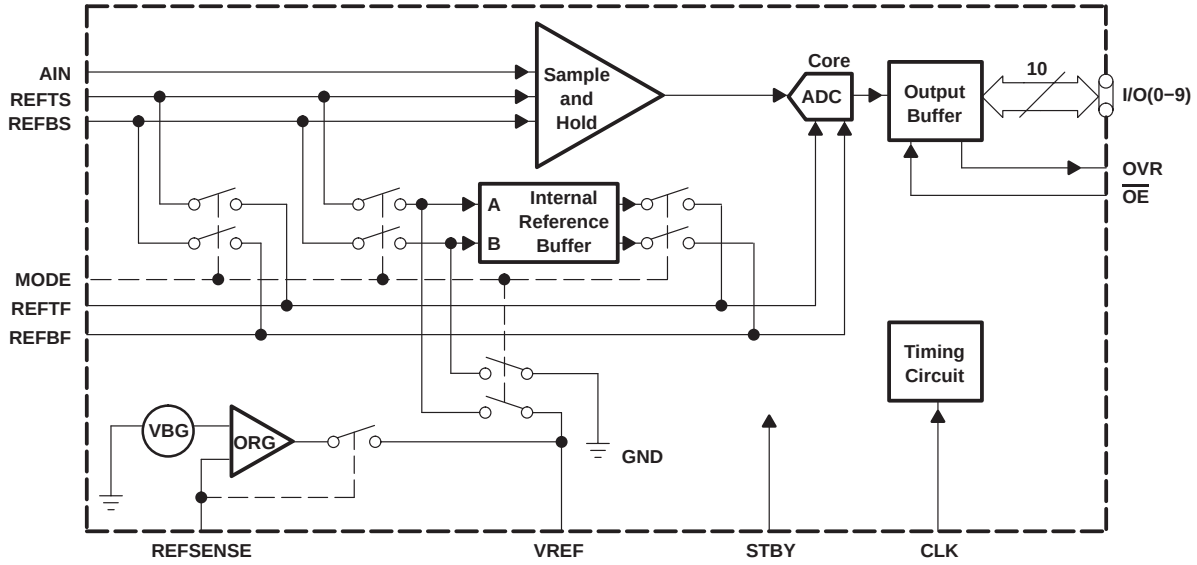
functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AGND	1, 19	I	Analog ground
AIN	27	I	Analog input
AV_{DD}	28	I	Analog supply
CLK	15	I	Clock input
DGND	14	I	Digital ground
DV_{DD}	2	I	Digital driver supply
I/O0	3	O	Digital I/O bit 0 (LSB)
I/O1	4		Digital I/O bit 1
I/O2	5		Digital I/O bit 2
I/O3	6		Digital I/O bit 3
I/O4	7		Digital I/O bit 4
I/O5	8		Digital I/O bit 5
I/O6	9		Digital I/O bit 6
I/O7	10		Digital I/O bit 7
I/O8	11		Digital I/O bit 8
I/O9	12		Digital I/O bit 9 (MSB)
MODE	23	I	Mode input
$\overline{OE}$	16	I	High to 3-state the data bus, low to enable the data bus
OVR	13	O	Out-of-range indicator
REFBS	25	I	Reference bottom sense
REFBF	24	I	Reference bottom decoupling
REFSENSE	18	I	Reference sense
REFTF	22	I	Reference top decoupling
REFTS	21	I	Reference top sense
STBY	17	I	High = power-down mode, low = normal operation mode
VREF	26	I/O	Internal and external reference
$\overline{876M}$	20	I	High = THS1030 mode, low = TLC876 mode (see section 4 for TLC876 mode)

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range: AV_{DD} to AGND, DV_{DD} to DGND . . . . . −0.3 V to 6.5 V
AGND to DGND . . . . . −0.3 V to 0.3 V
AV_{DD} to DV_{DD} . . . . . −6.5 V to 6.5 V
Mode input voltage range, MODE to AGND . . . . . −0.3 V to AV_{DD} + 0.3 V
Reference voltage input range, REFTF, REFTB, REFTS, REFBS to AGND . . . . . −0.3 V to AV_{DD} + 0.3 V
Analog input voltage range, AIN to AGND . . . . . −0.3 V to AV_{DD} + 0.3 V
Reference input voltage range, VREF to AGND . . . . . −0.3 V to AV_{DD} + 0.3 V
Reference output voltage range, VREF to AGND . . . . . −0.3 V to AV_{DD} + 0.3 V
Clock input voltage range, CLK to AGND . . . . . −0.3 V to AV_{DD} + 0.3 V
Digital input voltage range, digital input to DGND . . . . . −0.3 V to DV_{DD} + 0.3 V
Digital output voltage range, digital output to DGND . . . . . −0.3 V to DV_{DD} + 0.3 V
Operating junction temperature range, T_J . . . . . 0°C to 150°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 in) from case for 10 seconds . . . . . 300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

digital inputs

		MIN	NOM	MAX	UNIT
High-level input voltage, V_{IH}	Clock input	$0.8 \times AV_{DD}$			V
	All other inputs	$0.8 \times DV_{DD}$			
Low-level input voltage, V_{IL}	Clock input			$0.2 \times AV_{DD}$	V
	All other inputs			$0.2 \times DV_{DD}$	

analog inputs

		MIN	NOM	MAX	UNIT
Analog input voltage, $V_{I(AIN)}$		REFBS		REFTS	V
Reference input voltage	$V_{I(VREF)}$	1		2	V
	$V_{I(REFTS)}$	1		AV_{DD}	V
	$V_{I(REFBS)}$	0		$AV_{DD}-1$	V

power supply

			MIN	NOM	MAX	UNIT
Supply voltage	Maximum sampling rate = 30 MSPS	AV_{DD}	3	3.3	5.5	V
		DV_{DD}	3	3.3	5.5	

REFTS, REFBS reference voltages (MODE = AV_{DD})

		MIN	NOM	MAX	UNIT
Reference input voltage (top)	REFTS	1		AV_{DD}	V
Reference input voltage (bottom)	REFBS	0		$AV_{DD}-1$	V
Differential input voltage (REFTS − REFBS)		1		2	V
Switched sampling input capacitance on REFTS or REFBS			0.6		pF

recommended operating conditions (continued)

sampling rate and resolution

PARAMETER		MIN	NOM	MAX	UNIT
f_S	Sample frequency	5		30	MSPS
	Resolution		10		Bits

electrical characteristics over recommended operating conditions, AV_{DD} = 3 V, DV_{DD} = 3 V, f_S = 30 MSPS/50% duty cycle, MODE = AV_{DD}, 2-V input span from 0.5 V to 2.5 V, external reference, $T_A = T_{min}$ to T_{max} (unless otherwise noted)

analog inputs

PARAMETER		MIN	TYP	MAX	UNIT
$V_{I(AIN)}$	Analog input voltage	REFBS		REFTS	V
C_I	Switched sampling input capacitance		1.2		pF
BW	Full power bandwidth (−3 dB)		150		MHz
I_{lkg}	DC leakage current (input = ±FS)		60		µA

VREF reference voltages

PARAMETER	MIN	TYP	MAX	UNIT
Internal 1-V reference voltage (REFSENSE = VREF)	0.95	1	1.05	V
Internal 2-V reference voltage (REFSENSE = AGND)	1.90	2	2.10	V
External reference voltage (REFSENSE = AV_{DD})	1		2	V
Reference input resistance		680		Ω

REFTF, REFBF reference voltages

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Differential input voltage (REFTF − REFBF) (REFSENSE = VREF)			0.9	1	1.1	V
Differential input voltage (REFTF − REFBF) (REFSENSE = AGND)			1.9	2	2.1	V
Input common mode voltage (REFTF + REFBF)/2		AV_{DD} = 3 V	1.3	1.5	1.7	V
		AV_{DD} = 5 V	2	2.5	3	
REFTF voltage (MODE = AV_{DD})	VREF = 1 V	AV_{DD} = 3 V		2		V
		AV_{DD} = 5 V		3		
	VREF = 2 V	AV_{DD} = 3 V		2.5		V
		AV_{DD} = 5 V		3.5		
REFBF voltage (MODE = AV_{DD})	VREF = 1 V	AV_{DD} = 3 V		1		V
		AV_{DD} = 5 V		2		
	VREF = 2 V	AV_{DD} = 3 V		0.5		V
		AV_{DD} = 5 V		1.5		
Input resistance between REFTF and REFBF				600		Ω
Power up time for valid ADC conversions (t_{PUconv})		See Note 1		1.2		µs

NOTES: 1. Time from control register STBY pin returning low to the ADC conversion to be accurate within 0.1% of fullscale.

electrical characteristics over recommended operating conditions, AV_{DD} = 3 V, DV_{DD} = 3 V, f_S = 30 MSPS/50% duty cycle, MODE = AV_{DD}, 2-V input span from 0.5 V to 2.5 V, external reference, $T_A = T_{min}$ to T_{max} (unless otherwise noted) (continued)

dc accuracy

PARAMETER		MIN	TYP	MAX	UNIT
INL	Integral nonlinearity (see Note 2)		±1	±2	LSB
DNL	Differential nonlinearity (see Note 3)		±0.3	±1	LSB
	Offset error (see Note 4)		0.4	1.4	%FSR
	Gain error (see Note 5)		1.4	3.5	%FSR
	Missing code	No missing code assured			

NOTES: 2. Integral nonlinearity refers to the deviation of each individual code from a line drawn from zero to full scale. The point used as zero occurs 1/2 LSB before the first code transition. The full-scale point is defined as a level 1/2 LSB beyond the last code transition. The deviation is measured from the center of each particular code to the true straight line between these two endpoints.

3. An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. Therefore this measure indicates how uniform the transfer function step sizes are. The ideal step size is defined here as the step size for the device under test (i.e., (last transition level – first transition level) ÷ $(2^n – 2)$). Using this definition for DNL separates the effects of gain and offset error. A minimum DNL better than –1 LSB ensures no missing codes.

4. Offset error is defined as the difference in analog input voltage – between the ideal voltage and the actual voltage – that will switch the ADC output from code 0 to code 1. The ideal voltage level is determined by adding the voltage corresponding to 1/2 LSB to the bottom reference level. The voltage corresponding to 1 LSB is found from the difference of top and bottom references divided by the number of ADC output levels (1024).

5. Gain error is defined as the difference in analog input voltage – between the ideal voltage and the actual voltage – that will switch the ADC output from code 1022 to code 1023. The ideal voltage level is determined by subtracting the voltage corresponding to 1.5 LSB from the top reference level. The voltage corresponding to 1 LSB is found from the difference of top and bottom references divided by the number of ADC output levels (1024).

dynamic performance (See Note 6)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ENOB	Effective number of bits	f = 3.5 MHz	8.4	9		Bits
		f = 3.5 MHz, AV_{DD} = 5 V		9		
		f = 15 MHz, 3 V		7.8		
		f = 15 MHz, AV_{DD} = 5 V		7.7		
SFDR	Spurious free dynamic range	f = 3.5 MHz	56	60.6		dB
		f = 3.5 MHz, AV_{DD} = 5 V		64.6		
		f = 15 MHz		48.5		
		f = 15 MHz, AV_{DD} = 5 V		53		
THD	Total harmonic distortion	f = 3.5 MHz		−60	−56	dB
		f = 3.5 MHz, AV_{DD} = 5 V		−66.9		
		f = 15 MHz		−47.5		
		f = 15 MHz, AV_{DD} = 5 V		−53.1		
SNR	Signal-to-noise ratio	f = 3.5 MHz	53	57		dB
		f = 3.5 MHz, AV_{DD} = 5 V		56		
		f = 15 MHz		53.1		
		f = 15 MHz, AV_{DD} = 5 V		49.4		
SINAD	Signal-to-noise and distortion	f = 3.5 MHz	52.5	56		dB
		f = 3.5 MHz, AV_{DD} = 5 V		56		
		f = 15 MHz		48.6		
		f = 15 MHz, AV_{DD} = 5 V		48.1		

NOTES: 6. Input amplitude of single tone sine wave for dynamic tests is −0.5 dBFS.

electrical characteristics over recommended operating conditions, AV_{DD} = 3 V, DV_{DD} = 3 V, f_s = 30 MSPS/50% duty cycle, MODE = AV_{DD}, 2-V input span from 0.5 V to 2.5 V, external reference, $T_A = T_{min}$ to T_{max} (unless otherwise noted) (continued)

clock

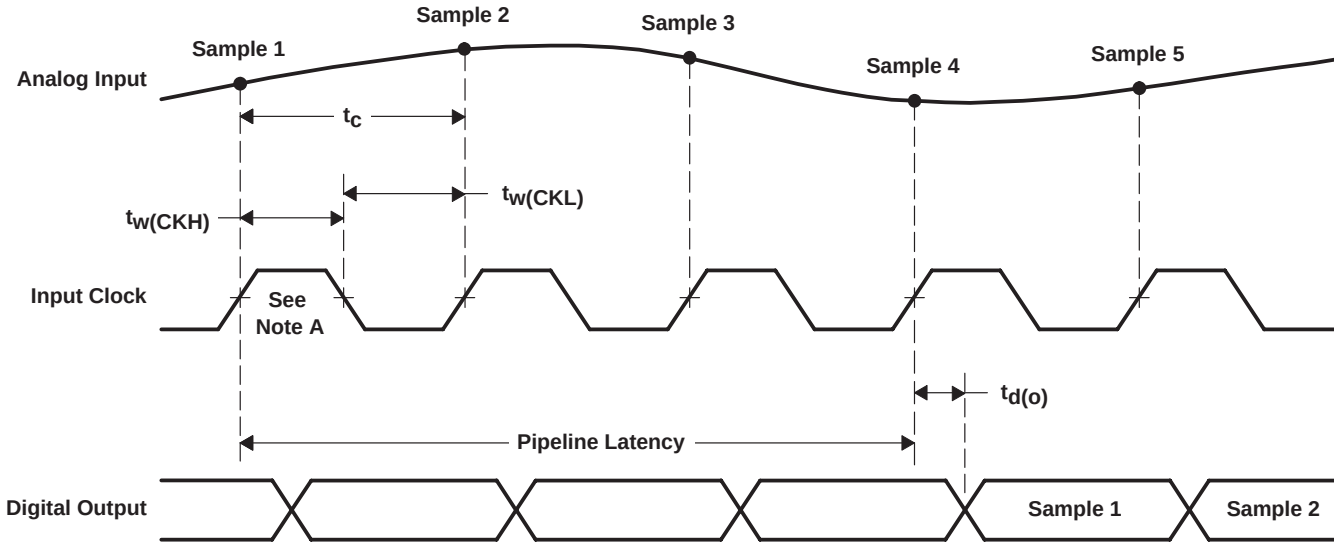
PARAMETER		MIN	TYP	MAX	UNIT
t_c	Clock cycle	33			ns
$t_{w(CKH)}$	Pulse duration, clock high	15	16.5	110	ns
$t_{w(CKL)}$	Pulse duration, clock low	15	16.5	110	ns
$t_{d(o)}$	Clock to data valid, delay time			25	ns
$t_{d(DZ)}$	Output disable to Hi-Z output, disable time			20	ns
$t_{d(DEN)}$	Output enable to output valid, enable time			20	ns
	Pipeline latency		3		Cycles
$t_{d(AP)}$	Aperture delay time		4		ns
	Aperture uncertainty (jitter)		2		ps

power supply (See Note 7)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Operating supply current	$AV_{DD} = DV_{DD}$ = 3 V, MODE = AVDD		29	40	mA
P_D	Power dissipation	$AV_{DD} = DV_{DD}$ = 3 V		87	120	mW
		$AV_{DD} = DV_{DD}$ = 5 V		150		
$P_{D(STBY)}$	Standby power	$AV_{DD} = DV_{DD}$ = 3 V, MODE = AVDD		3	5	mW

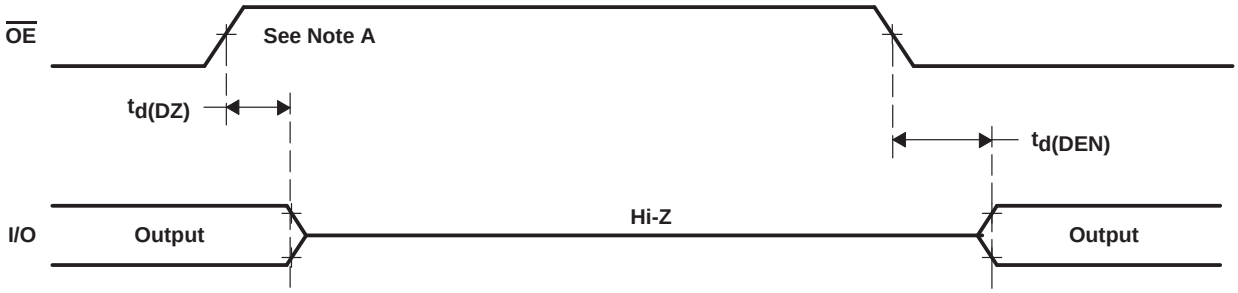
NOTES: 7. Mode and REFSENSE are set to AV_{DD}. The internal reference buffer is powered up to buffer the externally applied 0.5 V REFBS and 2.5 V REFTS. 1.5 VDC is applied at AIN while converting data at 30 MSPS.

PARAMETER MEASUREMENT INFORMATION



NOTE A: All timing measurements are based on 50% of edge transition.

Figure 1. Digital Output Timing Diagram



NOTE A: All timing measurements are based on 50% of edge transition.

Figure 2. Output Enable Timing Diagram

TYPICAL CHARACTERISTICS

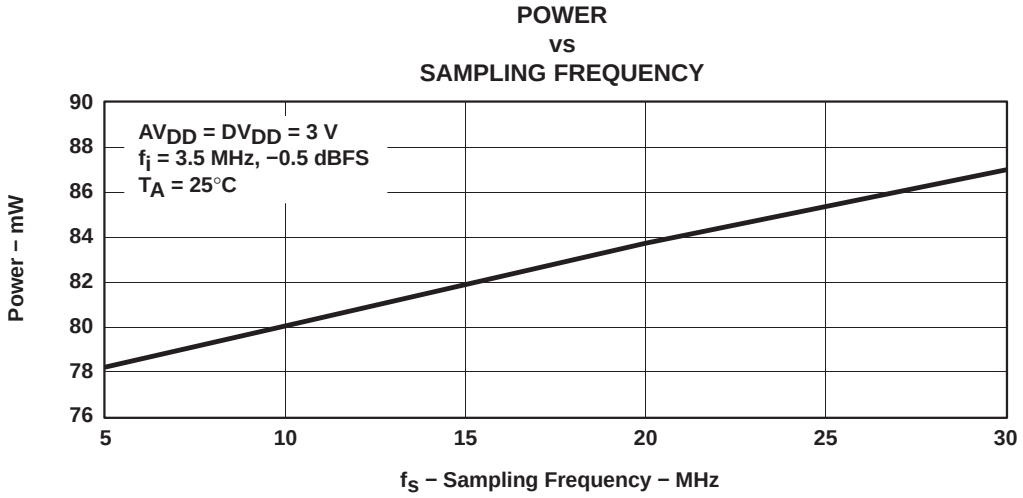


Figure 3

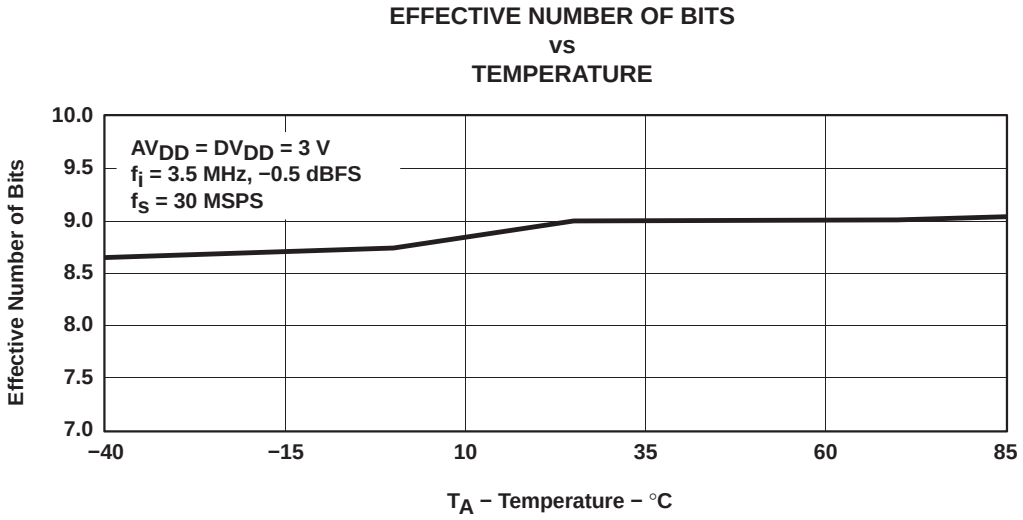


Figure 4

TYPICAL CHARACTERISTICS

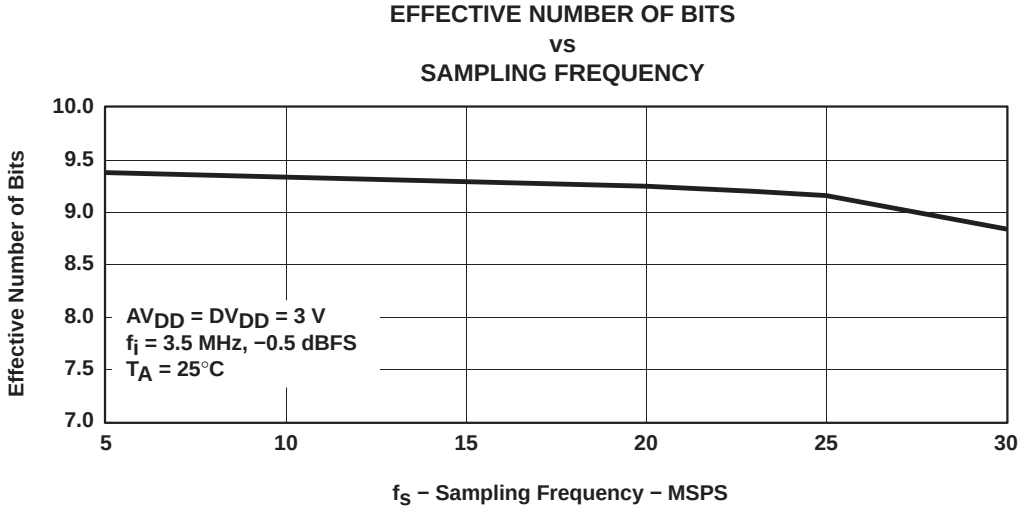


Figure 5

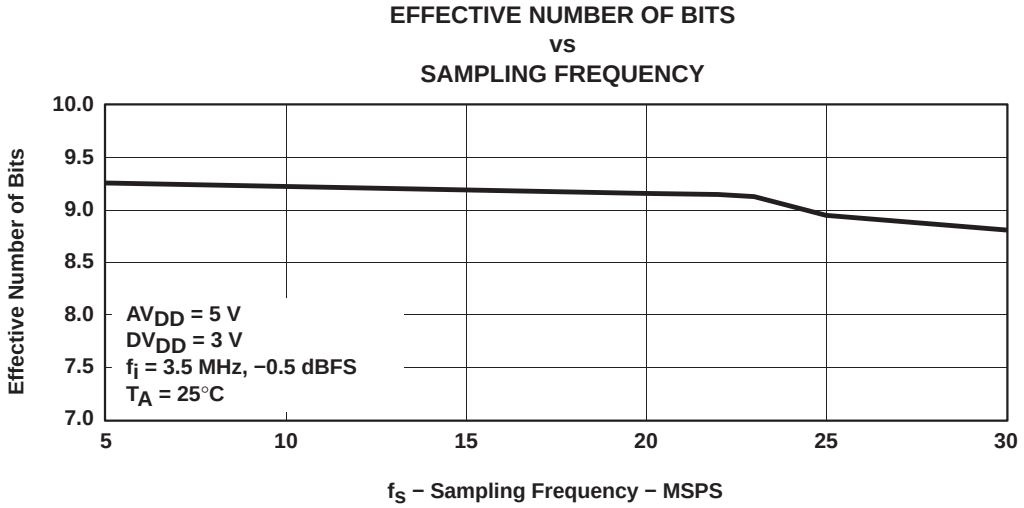


Figure 6

TYPICAL CHARACTERISTICS

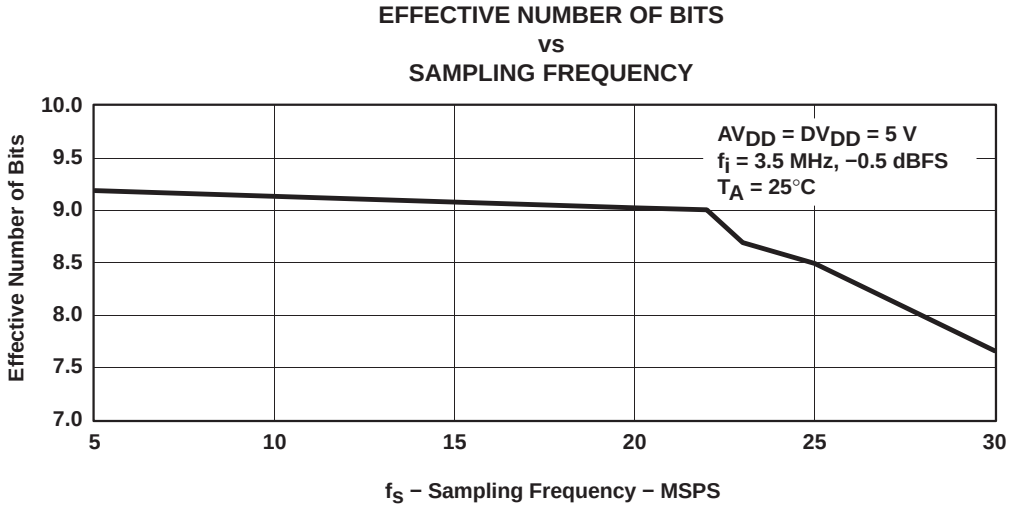


Figure 7

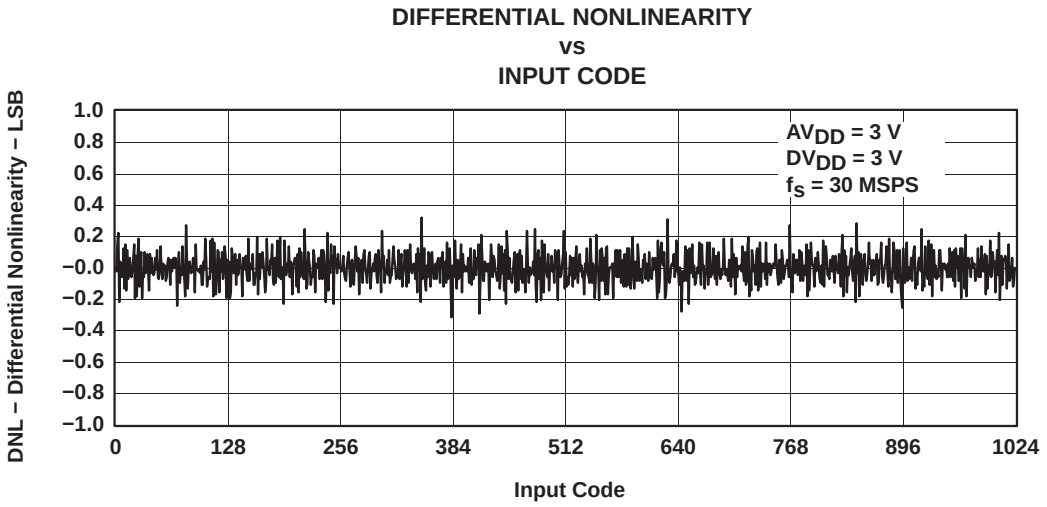


Figure 8

TYPICAL CHARACTERISTICS

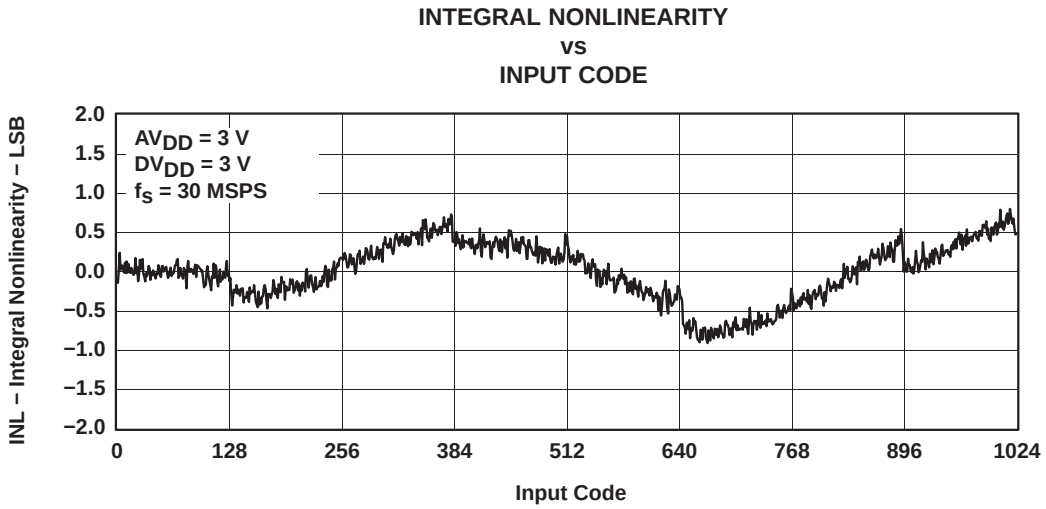


Figure 9

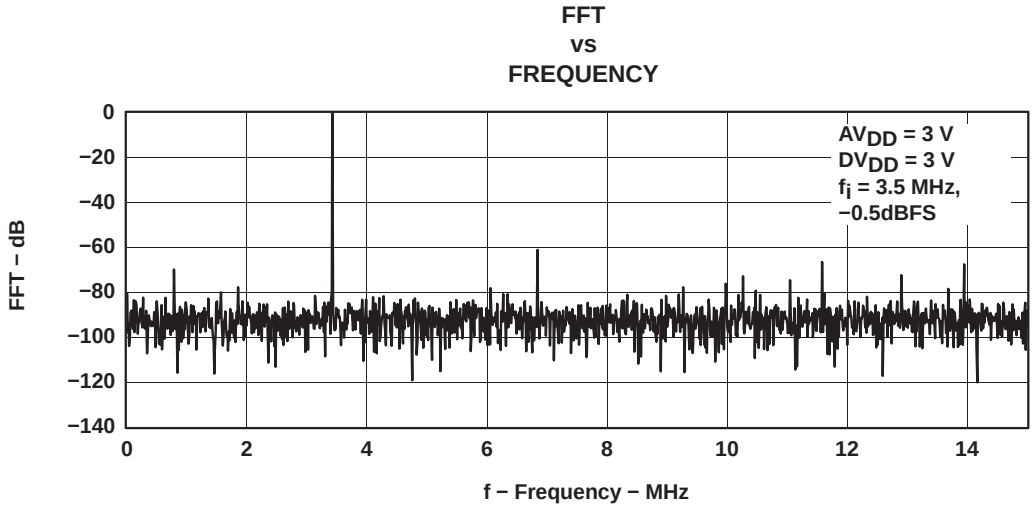


Figure 10

PRINCIPLES OF OPERATION

The analog input AIN is sampled in the sample and hold unit, the output of which feeds the ADC core, where the process of analog to digital conversion is performed against ADC reference voltages, REFTF and REFBF.

Connecting the MODE pin to one of three voltages, AGND, AV_{DD} or $AV_{DD}/2$ sets up operating configurations. The three settings open or close internal switches to select one of the three basic methods of ADC reference generation.

Depending on the user's choice of operating configuration, the ADC reference voltages may come from the internal reference buffer or may be fed from completely external sources. Where the reference buffer is employed, the user can choose to drive it from the onboard reference generator (ORG), or may use an external voltage source. A specific configuration is selected by connections to the REFSENSE, VREF, REFTS and REFBS, and REFTF and REFBF pins, along with any external voltage sources selected by the user.

The ADC core drives out through output buffers to the data pins D0 to D9. The output buffers can be disabled by the $\overline{OE}$ pin.

A single, sample-rate clock (30 MHz maximum) is required at pin CLK. The analog input signal is sampled on the rising edge of CLK, and corresponding data is output after following third rising edge.

The STBY pin controls the THS1030 power down.

The user-chosen operating configuration and reference voltages determine what input signal voltage range the THS1030 can handle.

The following sections explain:

- The internal signal flow of the device, and how the input signal span is related to the ADC reference voltages
- The ways in which the ADC reference voltages can be buffered internally, or externally applied
- How to set the onboard reference generator output, if required, and several examples of complete configurations

signal processing chain (sample and hold, ADC)

Figure 11 shows the signal flow through the sample and hold unit to the ADC core.

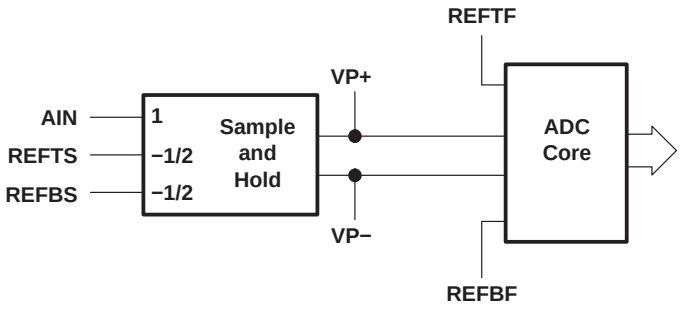


Figure 11. Analog Input Signal Flow

PRINCIPLES OF OPERATION

sample and hold

The analog input signal A_{IN} is applied to the AIN pin, either dc-coupled or ac-coupled.

The differential sample and hold processes A_{IN} with respect to the voltages applied to the REFTS and REFBS pins, to give a differential output $VP^{+} - VP^{-} = VP$ given by:

$$VP = A_{IN} - VM$$

Where:

$$VM = \frac{(REFTS + REFBS)}{2} \tag{1}$$

For single-ended input signals, VM is a constant voltage; usually the AIN mid-scale input voltage. However if MODE = $AV_{DD}/2$ then REFTS and REFBS can be connected together to operate with AIN as a complementary pair of differential inputs (see Figures 16 and 17).

analog-to-digital converter

In all operating configurations, VP is digitized against ADC reference voltages REFTF and REFBF, full-scale values of VP being given by:

$$VPFS + = \frac{+ (REFTF - REFBF)}{2} \tag{2}$$

$$VPFS - = \frac{- (REFTF - REFBF)}{2}$$

VP voltages outside the range VPFS− to VPFS+ lie outside the conversion range of the ADC. Attempts to convert out-of-range inputs are signaled to the application by driving the OVR output pin high. VP voltages less than VPFS− give ADC output code 0. VP voltages greater than VPFS+ give output code 1023.

complete system

Combining the above equations, the analog full scale input voltages at AIN which give VPFS+ and VPFS− at the sample and hold output are:

$$A_{IN} = FS + = VM + \frac{(REFTF - REFBF)}{2} \tag{3}$$

and

$$A_{IN} = FS - = VM - \frac{(REFTF - REFBF)}{2} \tag{4}$$

The analog input span (voltage range) that lies within the ADC conversion range is:

$$\text{Input span} = [(FS +) - (FS -)] = (REFTF - REFBF) \tag{5}$$

The REFTF and REFBF voltage difference sets the device input range. The next sections describe in detail the various methods available for setting voltages REFTF and REFBF to obtain the desired input span and ADC performance.

PRINCIPLES OF OPERATION

ADC reference generation

The THS1030 has three primary modes of ADC reference generation, selected by the voltage level applied to the MODE pin.

Connecting the MODE pin to AGND gives full external reference mode. In this mode, the user supplies the ADC reference voltages directly to pins REFTF and REFBF. This mode is used where there is need for minimum power drain or where there are very tight tolerances on the ADC reference voltages. This mode also offers the possibility of Kelvin connection of the reference inputs to the THS1030 to eliminate any voltage drops from remote references that may occur in the system. Only single-ended input is possible in this mode.

Connecting the MODE pin to $AV_{DD}/2$ gives differential mode. In this mode, the ADC reference voltages REFTF and REFBF are generated by the internal reference buffer from the voltage applied to the VREF pin. This mode is suitable for handling differentially presented inputs, which are applied to the AIN and REFTS/REFBS pins. A special case of differential mode is center span mode, in which the user applies a single-ended signal to AIN and applies the mid-scale input voltage (VM) to the REFTS and REFBS pins.

Connecting the MODE pin to AV_{DD} gives top/bottom mode. In this mode, the ADC reference voltages REFTF and REFBF are generated by the internal reference buffer from the voltages applied to the REFTS and REFBS pins. Only single-ended input is possible in top/bottom mode.

When MODE is connected to AGND, the internal reference buffer is powered down, its inputs and outputs disconnected, and REFTS and REFBS internally connected to REFTF and REFBF respectively. These nodes are connected by the user to external sources to provide the ADC reference voltages. The internal connections are designed for use in kelvin connection mode (Figure 14). When using external reference mode as shown in Figure 13, REFTS must be shorted to REFTF and REFBS must be shorted to REFBF externally. The mean of REFTF and REFBF must be equal to $AV_{DD}/2$. See Figure 13.

Table 1. Typical Set of Reference Connections

REFERENCE MODE	MODE	REFSENSE	VREF VOLTAGE	REFTS, REFBS	ANALOG INPUT	FIGURES
External	AGND	AV_{DD}	Disabled	Reference buffer powered down, reference voltage provided directly by REFT and REFB	Single-ended	12, 13, 14
Internal	$AV_{DD}/2$	VREF	1 V	Externally connect REFTS to REFBS. This pair then forms AIN− to the ADC.	Differential or center span	15, 16, 17
		AGND	2 V			
		External divider	1 + Ra/Rb (see Figure 22)			
External (through internal reference buffer)	AV_{DD}	AV_{DD}	Disabled	REFTS = V_{FS+} REFBS = V_{FS-}	Single-ended (top-bottom mode)	18, 19
Output of VREF can be externally tied to REFTS or REFBS to provide one of the reference voltages		VREF	1 V			
		AGND	2 V			
		External divider	1 + Ra/Rb (see Figure 22)			

PRINCIPLES OF OPERATION

full external reference mode (mode = AGND)

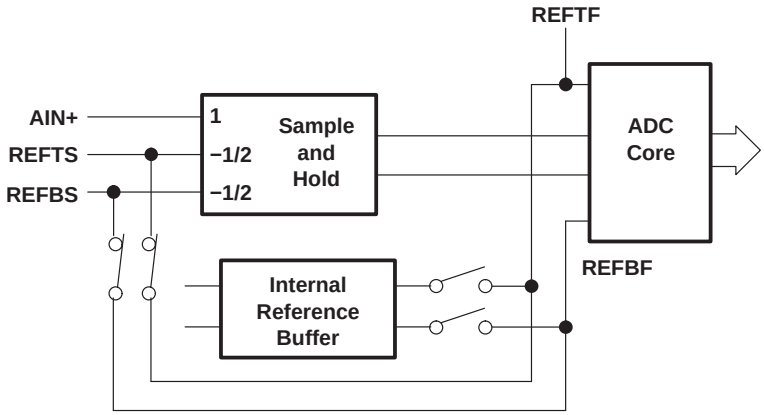


Figure 12. ADC Reference Generation, Full External Reference Mode (MODE = AGND)

It is also possible to use REFTS and REFBS as sense lines to drive the REFTF and REFBF lines (Kelvin mode) to overcome any voltage drops within the system. See Figure 14.

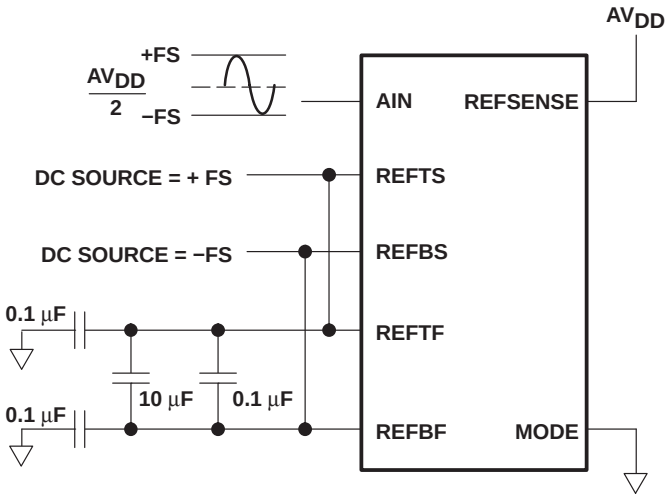


Figure 13. Full External Reference Mode

PRINCIPLES OF OPERATION

full external reference mode (mode = AGND) (continued)

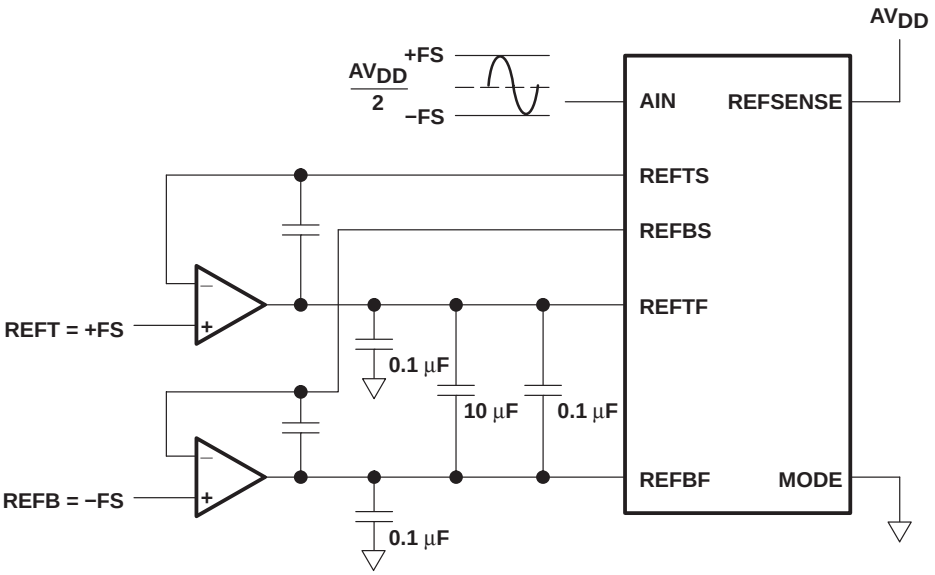


Figure 14. Full External Reference With Kelvin Connections

differential input mode (MODE = $AV_{DD}/2$)

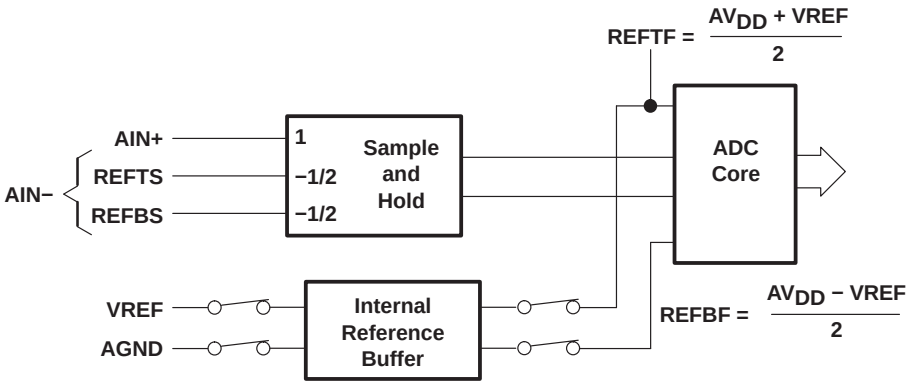


Figure 15. ADC Reference Generation, MODE = $AV_{DD}/2$

When MODE = $AV_{DD}/2$, the internal reference buffer is enabled, its outputs internally switched to REFTF and REFBF and inputs internally switched to VREF and AGND as shown in Figure 15. The REFTF and REFBF voltages are centered on $AV_{DD}/2$ by the internal reference buffer and the voltage difference between REFTF and REFBF equals the voltage at VREF. The internal REFTS to REFBS and REFTF to REFBF switches are open in this mode, allowing REFTS and REFBS to form the AIN− to the sample and hold.

Depending on the connection of the REFSENSE pin, the voltage on VREF may be externally driven, or set to an internally generated voltage of 1 V, 2 V, or an intermediate voltage (see the section on onboard reference generator configuration).

PRINCIPLES OF OPERATION

differential input mode (MODE = $AV_{DD}/2$) (continued)

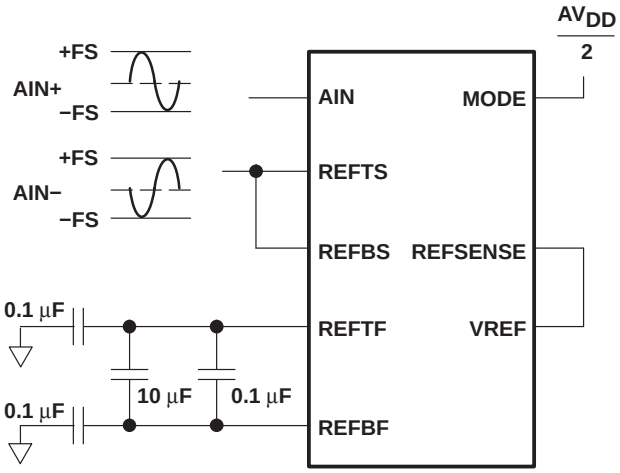


Figure 16. Differential Input Mode, 1-V Reference Span

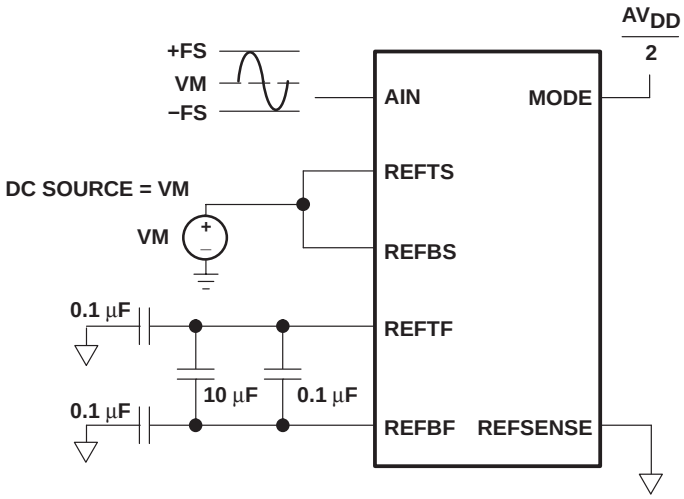


Figure 17. Center Span Mode, 2-V Reference Span

PRINCIPLES OF OPERATION

top/bottom mode (MODE = AV_{DD})

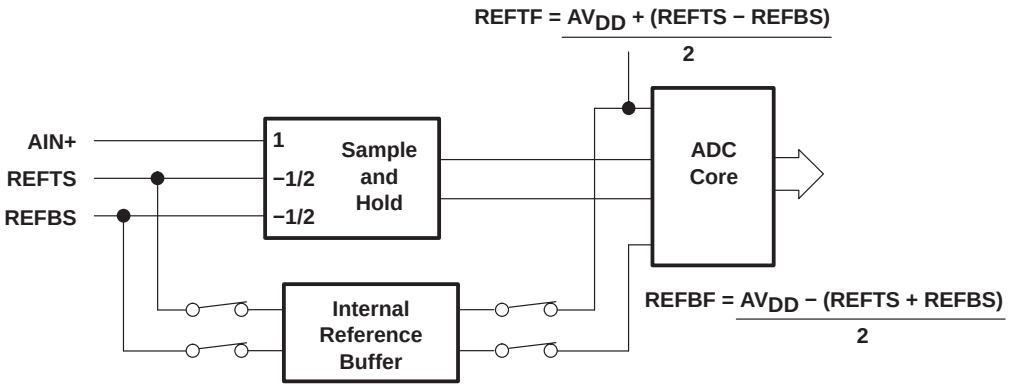


Figure 18. ADC Reference Generation Mode = AV_{DD}

Connecting MODE to AV_{DD} enables the internal reference buffer. Its inputs are internally switched to the REFTS and REFBS pins and its outputs internally switched to pins REFTF and REFBF. The internal connections (REFTS to REFTF) and (REFBS to REFBF) are broken.

The REFTS and REFBS voltages set the analog input span limits FS+ and FS− respectively. Any voltages at AIN greater than REFTS or less than REFBS will cause ADC over-range, which is signaled by OVR going high when the conversion result is output.

Typically, REFSENSE is tied to AV_{DD} to disable the ORG output to VREF (as in Figure 19), but the user can choose to use the ORG output to VREF as either REFTS or REFBS.

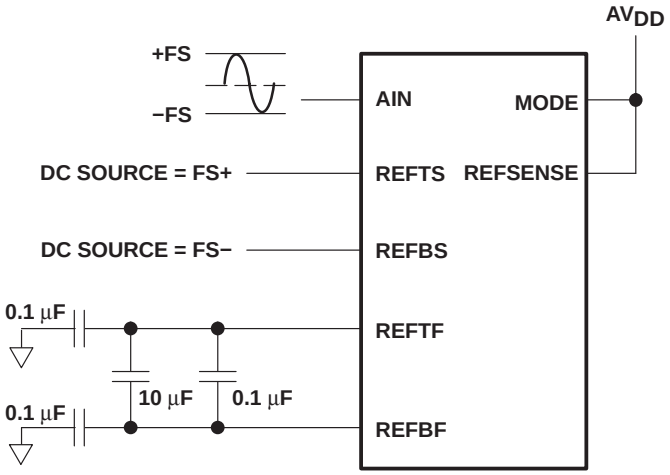


Figure 19. Top/Bottom Reference Mode

PRINCIPLES OF OPERATION

onboard reference generator configuration

The onboard reference generator (ORG) can provide a supply-voltage-independent and temperature-independent voltage on pin VREF.

External connections to REFSENSE control the ORG's output to the VREF pin as shown in Table 2.

Table 2. Effect of REFSENSE Connection on VREF Value

REFSENSE CONNECTION	ORG OUTPUT TO VREF	REFER TO:
VREF pin	1 V	Figure 20
AGND	2 V	Figure 21
External divider junction	$(1 + R_A/R_B)$	Figure 22
AV_{DD}	Open circuit	Figure 23

REFSENSE = AV_{DD} powers the ORG down, saving power when the ORG function is not required.

If MODE = $AV_{DD}/2$, the voltage on VREF determines the ADC reference voltages:

$$\mathrm{REFTF} = \frac{AV_{DD}}{2} + \frac{\mathrm{VREF}}{2} \qquad (6)$$

$$\mathrm{REFBF} = \frac{AV_{DD}}{2} - \frac{\mathrm{VREF}}{2}$$

$$\mathrm{REFTF} - \mathrm{REFBF} = \mathrm{VREF}$$

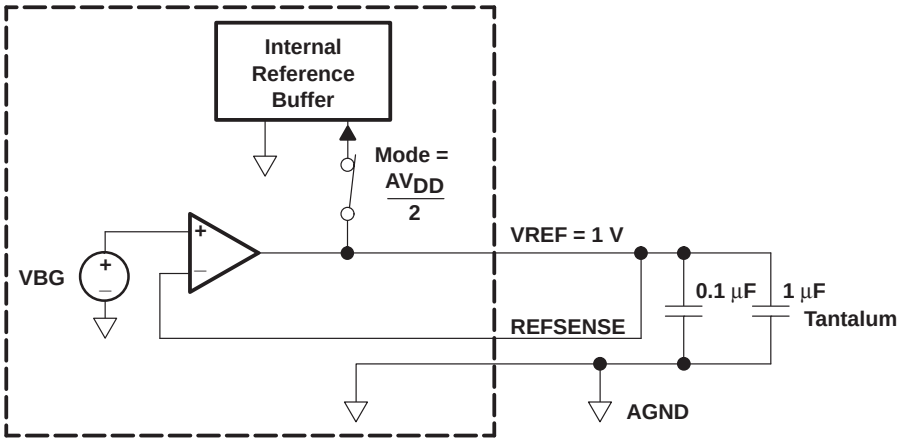


Figure 20. 1-V VREF Using ORG

PRINCIPLES OF OPERATION

onboard reference generator configuration (continued)

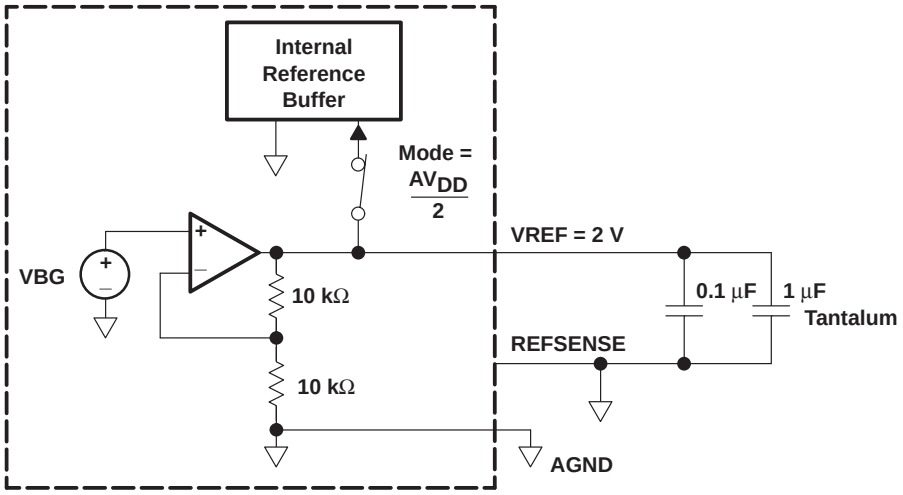


Figure 21. 2-V VREF Using ORG

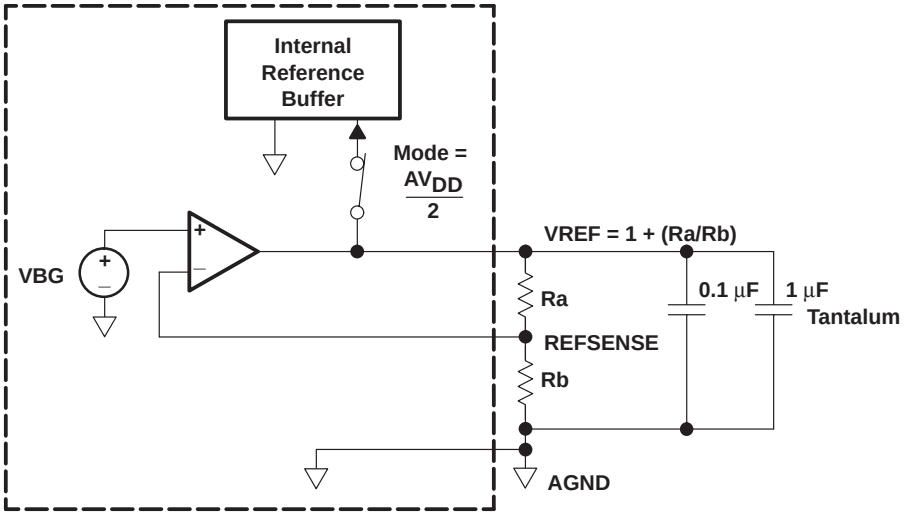


Figure 22. External Divider Mode

PRINCIPLES OF OPERATION

onboard reference generator configuration (continued)

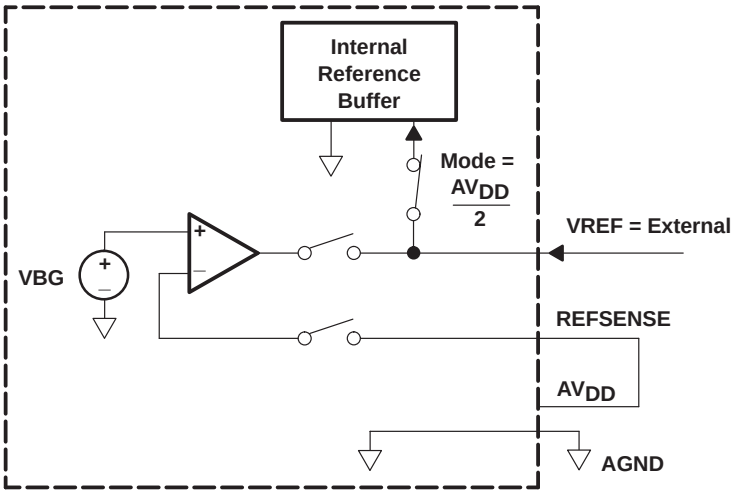


Figure 23. Drive VREF Mode

operating configuration examples

This section provides examples of operating configurations.

Figure 24 shows the operating configuration in top/bottom mode for a 2-V span single-ended input, using VREF to drive REFTS. Connecting the mode pin to AV_{DD} puts the THS1030 in top/bottom mode. Connecting pin REFSENSE to AGND sets the output of the ORG to 2 V. REFTS and REFBS are user-connected to VREF and AGND respectively to match the AIN pin input range to the voltage range of the input signal.

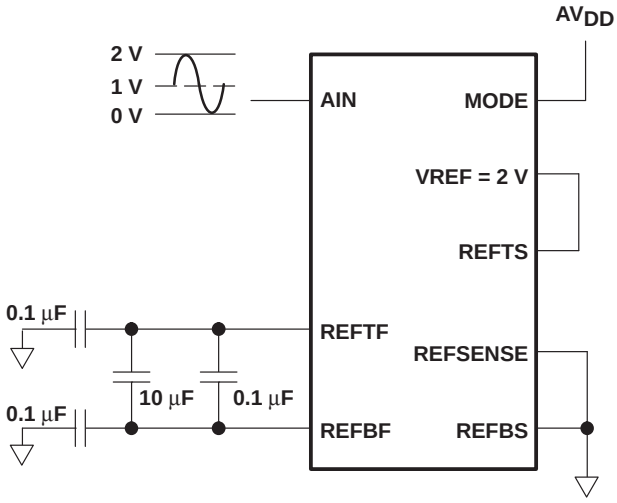


Figure 24. Operation Configuration in Top/Bottom Mode

In Figure 25 the input signal is differential, so mode = $AV_{DD}/2$ (differential mode) is set to allow the inverse signal to be applied to REFTS and REFBS. The differential input goes from −0.8 V to 0.8 V, giving a total input signal span of 1.6 V, REFTF−REFBF should therefore equal 1.6 V. REFSENSE is connected to resistors RA and RB (external divider mode) to make VREF = 1.6 V, that is R_A/R_B = 0.6 (see Figure 22).

PRINCIPLES OF OPERATION

operating configuration examples (continued)

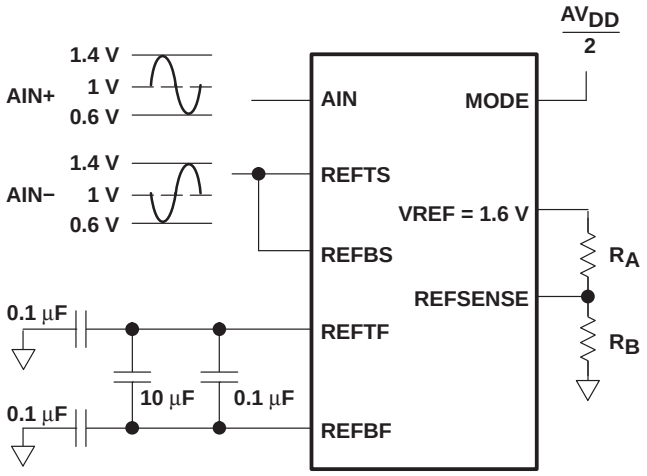


Figure 25. Differential Operation

Figure 26 shows a center span configuration for an input waveform swinging between 0.2 V and 1.9 V. Pins REFTS and REFBS are connected to a voltage source of 1.05 V, equal to the mid-scale of the input waveform. REFTF−REFBF should be set equal to the span of the input waveform, 1.7 V, so VREF is connected to an external source of 1.7 V. REFSENSE must be connected to AV_{DD} to disable the ORG output to VREF (see Figure 23) to allow this external source to be applied.

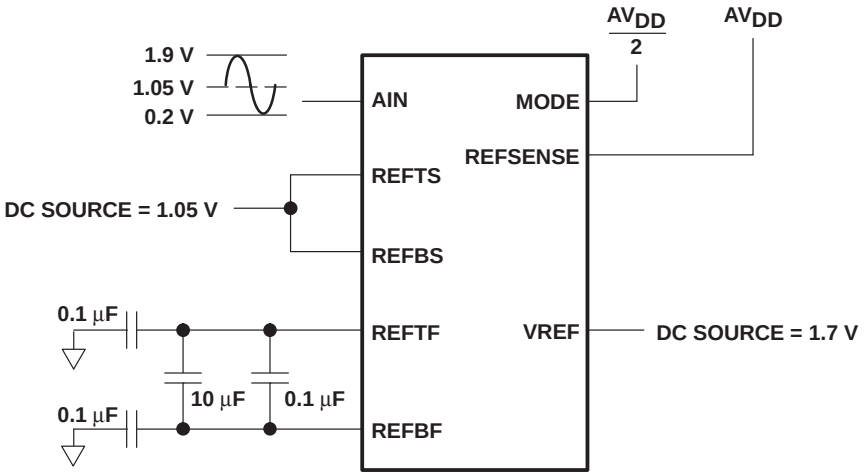


Figure 26. Center Span Operation

PRINCIPLES OF OPERATION

power management

In power-sensitive applications (such as battery-powered systems) where the THS1030 ADC is not required to convert continuously, power can be saved between conversion intervals by placing the THS1030 into power-down mode. This is achieved by setting pin 17 (STBY) to 1. In power-down mode, the device typically consumes less than 1 mW of power (from AV_{DD} and DV_{DD}) in either top/bottom mode or center-span mode. On power up, the THS1030 typically requires 5 ms of wake-up time before valid conversion results are available in either top/bottom or center span modes.

Disabling the ORG in applications where the ORG output is not required can also reduce power dissipation by 1 mA analog I_{DD}. This is achieved by connecting the REFSENSE pin to AV_{DD}.

output format and digital I/O

While the $\overline{OE}$ pin is held low, ADC conversion results are output at pins D0 (LSB) to D9 (MSB). The ADC input over-range indicator is output at pin OVR. OVR is also disabled when $\overline{OE}$ is held high.

The ADC output data format is unsigned binary (output codes 0 to 1023).

driving the THS1030 analog inputs

driving AIN

Figure 26 shows an equivalent circuit for the THS1030 AIN pin. The load presented to the system at the AIN pin comprises the switched input sampling capacitor, C_{SAMPLE}, and various stray capacitances, C_{P1} and C_{P2}.

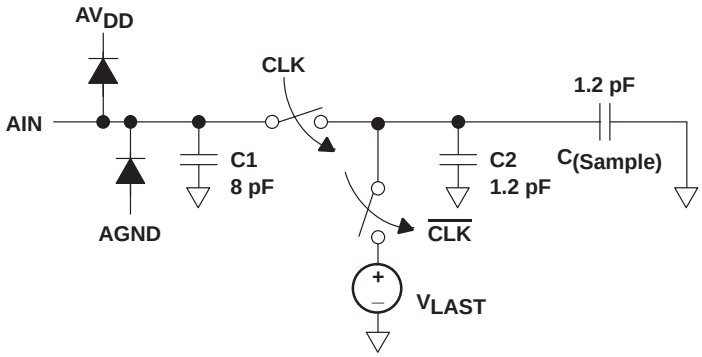


Figure 27. Equivalent Circuit of Analog Input AIN

In any single-ended input mode, V_{LAST} = the average of the previously sampled voltage at AIN and the average of the voltages on pins REFTS and REFBS. In any differential mode, V_{LAST} = the common mode input voltage.

The external source driving AIN must be able to charge and settle into C_{SAMPLE} and the C_{P1} and C_{P2} strays to within 0.5 LSB error while sampling (CLK pin low) to achieve full ADC resolution.

PRINCIPLES OF OPERATION

AIN input current and input load modeling

When CLK goes low, the source driving AIN must charge the total switched capacitance $C_S = C_{SAMPLE} + C_{P2}$. The total charge transferred depends on the voltage at AIN and is given by:

$$Q_{CHARGING} = (AIN - V_{LAST}) \times C_S. \tag{7}$$

For a fixed voltage at AIN, so that AIN and V_{LAST} do not change between samples, the maximum amount of charge transfer occurs at AIN = FS− (charging current flows out of THS1030) and AIN = FS+ (current flows into THS1030). If AIN is held at the voltage FS+, V_{LAST} = [(FS+) + VM]/2, giving a maximum transferred charge:

$$Q(FS) = \frac{(FS+) - [(FS+) + VM]}{2} \times C_S = \frac{[(FS+) - VM] \times C_S}{2} \tag{8}$$

$$= (1/4 \text{ of the input voltage span}) \times C_S$$

If the input voltage changes between samples, then the maximum possible charge transfer is

$$Q(max) = 3 \times Q(FS) \tag{9}$$

which occurs for a full-scale input change (FS+ to FS− or FS− to FS+) between samples.

The charging current pulses can make the AIN source jump or ring, especially if the source is slightly inductive at high frequencies. Inserting a small series resistor of 20 Ω or less in the input path can damp source ringing (see Figure 31). This resistor can be made larger than 20 Ω if reduced input bandwidth or distortion performance is acceptable.

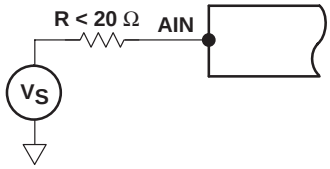


Figure 28. Damping Source Ringing Using a Small Resistor

PRINCIPLES OF OPERATION

equivalent input resistance at AIN and ac-coupling to AIN

Some applications may require ac-coupling of the input signal to the AIN pin. Such applications can use an ac-coupling network such as shown in Figure 29.

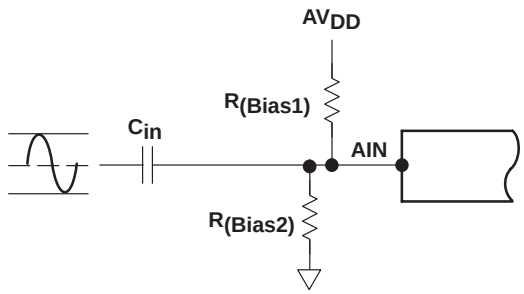


Figure 29. AC-Coupling the Input Signal to the AIN Pin

Note that if the bias voltage is derived from the supplies, as shown in Figure 29, then additional filtering should be used to ensure that noise from the supplies does not reach AIN.

Working with the input current pulse equations given in the previous section is awkward when designing ac-coupling input networks. For such design, it is much simpler to model the AIN input as an equivalent resistance, R_{AIN}, from the AIN pin to a voltage source VM where

$$VM = (REFTS + REFBS)/2 \text{ and } R_{AIN} = 1 / (C_S \times f_{clk})$$

where f_{clk} is the CLK frequency.

The high-pass −3 dB cutoff frequency for the circuit shown in Figure 29 is:

$$f_{(-3\ dB)} = \frac{1}{\left(2 \times \pi \times R_{IN}tot\right)} \tag{10}$$

where R_{IN}tot is the parallel combination of Rbias1, Rbias2, and R_{AIN}. This approximation is good provided that the clock frequency, f_{clk}, is much higher than f(−3 dB).

Note also that the effect of the equivalent R_{AIN} and VM at the AIN pin must be allowed for when designing the bias network dc level.

details

The above value for R_{AIN} is derived by noting that the average AIN voltage must equal the bias voltage supplied by the ac coupling network. The average value of V_{LAST} in equation 8 is thus a constant voltage

$$V_{LAST} = V(\text{AIN bias}) - VM$$

For an input voltage Vin at the AIN pin,

$$Qin = (Vin - V_{LAST}) \times Cs$$

Provided that f (−3 dB) is much lower than f_{clk}, a constant current flowing over the clock period can approximate the input charging pulse

$$\begin{aligned} Iin &= Qin / t_{clk} \\ &= Qin \times f_{clk} \\ &= (Vin - V_{LAST}) \times C_S \times f_{clk} \end{aligned}$$

PRINCIPLES OF OPERATION

details (continued)

The ac input resistance R_{AIN} is then

$$R_{AIN} = dIin / dVin$$
$$= 1 / (dVin / dIin)$$
$$= 1 / (C_S \times f_{clk})$$

driving the VREF pin (differential mode)

Figure 30 shows the equivalent load on the VREF pin when driving the internal reference buffer via this pin (MODE = $AV_{DD}/2$ and REFSENSE = AV_{DD}).

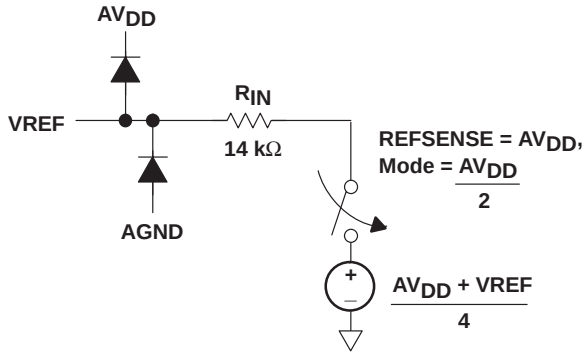


Figure 30. Equivalent Circuit of VREF

The current flowing into I_{IN} is given by

$$I_{IN} = \frac{\left(3 \times VREF - AV_{DD}\right)}{\left(4 \times R_{IN}\right)} \tag{11}$$

Note that the actual I_{IN} may differ from this value by up to ±50% due to device-to-device processing variations and allowing for operating temperature variations.

The user should ensure that VREF is driven from a low noise, low drift source, well-decoupled to analog ground and capable of driving I_{IN}.

PRINCIPLES OF OPERATION

driving the internal reference buffer (top/bottom mode)

Figure 31 shows the load present on the REFTS and REFBS pins in top/bottom mode due to the internal reference buffer only. The sample and hold must also be driven via these pins, which adds additional load.

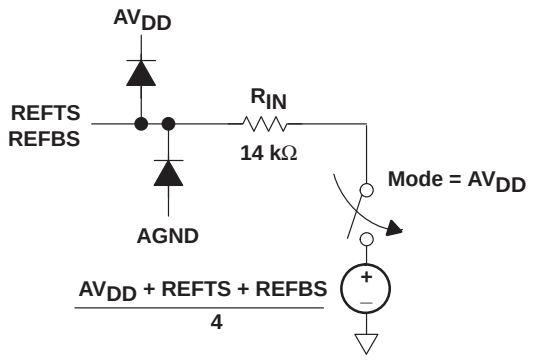


Figure 31. Equivalent Circuit of Inputs to Internal Reference Buffer

Equations for the currents flowing into REFTS and REFBS are:

$$I_{IN}TS = \frac{\left(3 \times REFTS - AV_{DD} - REFBS\right)}{\left(4 \times R_{IN}\right)} \tag{12}$$

$$I_{IN}BS = \frac{\left(3 \times REFBS - AV_{DD} - REFTS\right)}{\left(4 \times R_{IN}\right)} \tag{13}$$

These currents must be provided by the sources on REFTS and REFBS in addition to the requirements of driving the sample and hold. Tolerance on these currents are ±50%.

driving REFTS and REFBS

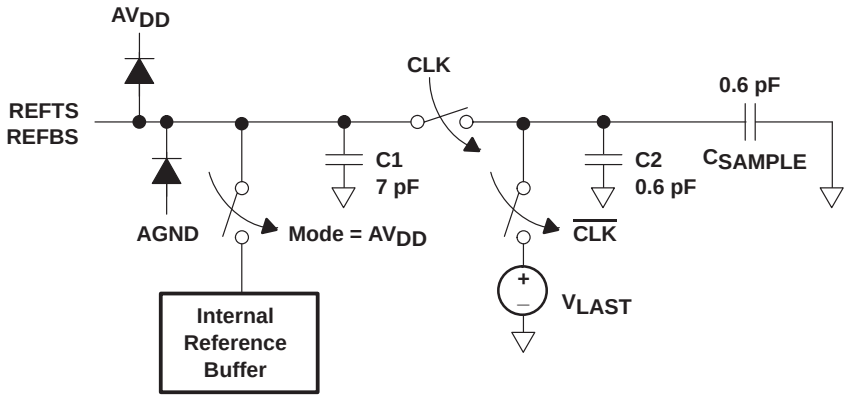


Figure 32. Equivalent Circuit of REFTS and REFBS Inputs

This is essentially a combination of driving the ADC internal reference buffer (if in top/bottom mode) and also driving a switched capacitor load like AIN, but with the sampling capacitor and C_{P2} on each pin now being 0.6 pF and about 0.6 pF respectively.

PRINCIPLES OF OPERATION

driving REFTF and REFBF (full external reference mode)

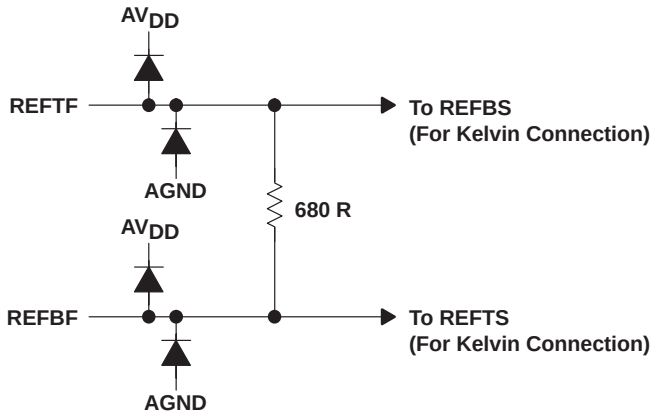


Figure 33. Equivalent Circuit of REFTF and REFBF Inputs

Note the need for off-chip decoupling.

driving the clock input

Obtaining good performance from the THS1030 requires care when driving the clock input.

Different sections of the sample-and-hold and ADC operate while the clock is low or high. The user should ensure that the clock duty cycle remains near 50% to ensure that all internal circuits have as much time as possible in which to operate.

The CLK pin should be driven from a low jitter source for best dynamic performance. To maintain low jitter at the CLK input, any clock buffers external to the THS1030 should have fast rising edges. Use a fast logic family such as AC or ACT to drive the CLK pin, and consider powering any clock buffers separately from any other logic on the PCB to prevent digital supply noise appearing on the buffered clock edges as jitter.

The CLK input threshold is nominally around $AV_{DD}/2$—ensure that any clock buffers have an appropriate supply voltage to drive above and below this level.

digital output loading and circuit board layout

The THS1030 outputs are capable of driving rail-to-rail with up to 20 pF of load per pin at 30-MHz clock and 3-V digital supply. Minimizing the load on the outputs will improve THS1030 signal-to-noise performance by reducing the switching noise coupling from the THS1030 output buffers to the internal analog circuits. The output load capacitance can be minimized by buffering the THS1030 digital outputs with a low input capacitance buffer placed as close to the output pins as physically possible, and by using the shortest possible tracks between the THS1030 and this buffer.

Noise levels at the output buffers, and hence coupling to the analog circuits within THS1030, becomes worse as the THS1030 digital supply voltage is increased. Where possible, consider using the lowest DV_{DD} that the application can tolerate.

Use good layout practices when designing the application PCB to ensure that any off-chip return currents from the THS1030 digital outputs (and any other digital circuits on the PCB) do not return via the supplies to any sensitive analog circuits. The THS1030 should be soldered directly to the PCB for best performance. Socketing the device will degrade performance by adding parasitic socket inductance and capacitance to all pins.

PRINCIPLES OF OPERATION

user tips for obtaining best performance from the THS1030

- Voltages on AIN, REFTF and REFBF and REFTS and REFBS must all be inside the supply rails.
- ORG modes offer the simplest configurations for ADC reference generation.
- Choose differential input mode for best distortion performance.
- Choose a 2-V ADC input span for best noise performance.
- Choose a 1-V ADC input span for best distortion performance.
- If the ORG is not used to provide ADC reference voltages, its output may be used for other purposes in the system. Care should be taken to ensure noise is not injected into the THS1030.
- Use external voltage sources for ADC reference generation where there are stringent requirements on accuracy and drift.
- Drive clock input CLK from a low-jitter, fast logic stage, with a well-decoupled power supply and short PCB traces.

TLC876 mode

The THS1030 is pin compatible with the TI TLC876 and thus enables users of TLC876 to upgrade to higher speed by dropping the THS1030 into their sockets. Grounding the 1876M pin effectively puts the THS1030 into 876 mode using the external ADC reference. The MODE pin should either be grounded or left floating.

The REFSENSE pin is connected to DV_{DD} when the THS1030 is dropped into a TLC876 socket. For DV_{DD} = 5-V applications, this will disable the ORG. For TLC876 applications using DV_{DD} = 3.3 V, the VREF pin will be driven to AV_{SS}. In TLC876/AD876 mode, the pipeline latency is increased to 3.5 clock cycles to match the TLC876 latency.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
THS1030CDW	OBSOLETE	SOIC	DW	28		TBD	Call TI	Call TI	0 to 70	TH1030	
THS1030CDWG4	OBSOLETE	SOIC	DW	28		TBD	Call TI	Call TI	0 to 70		
THS1030CDWR	OBSOLETE	SOIC	DW	28		TBD	Call TI	Call TI	0 to 70	TH1030	
THS1030CPW	ACTIVE	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TH1030	Samples
THS1030CPWR	ACTIVE	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TH1030	Samples
THS1030IDW	OBSOLETE	SOIC	DW	28		TBD	Call TI	Call TI	-40 to 85	TJ1030	
THS1030IPW	ACTIVE	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TJ1030	Samples
THS1030IPWR	ACTIVE	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TJ1030	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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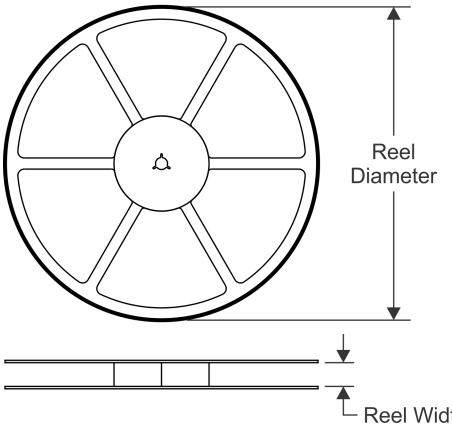
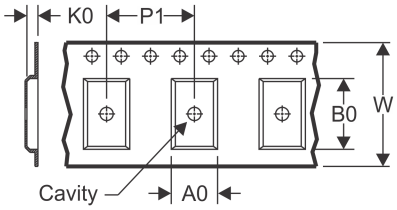
TAPE AND REEL INFORMATION

REEL DIMENSIONS

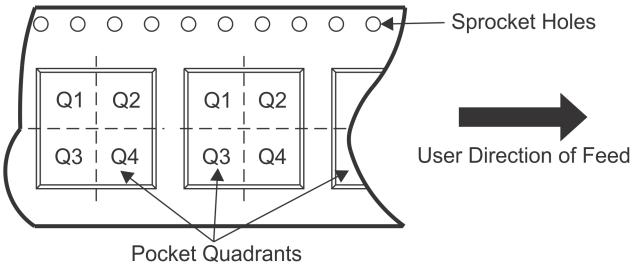


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

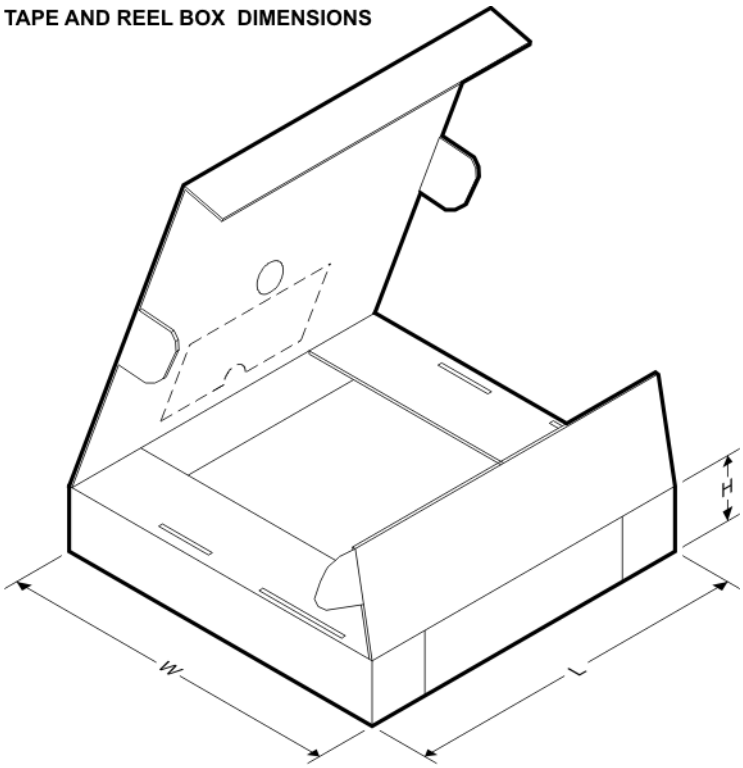
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS1030CPWR	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
THS1030IPWR	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

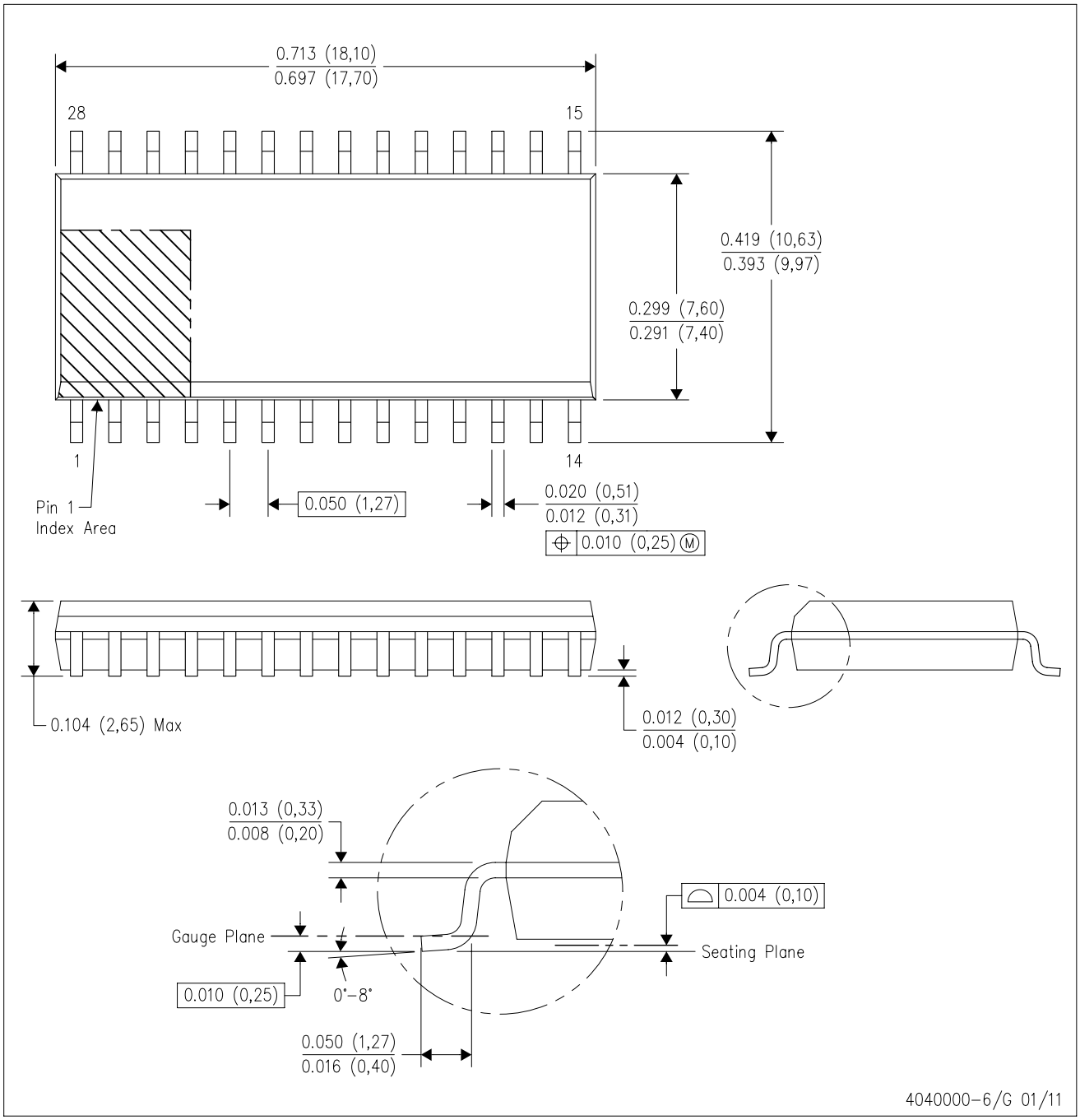
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

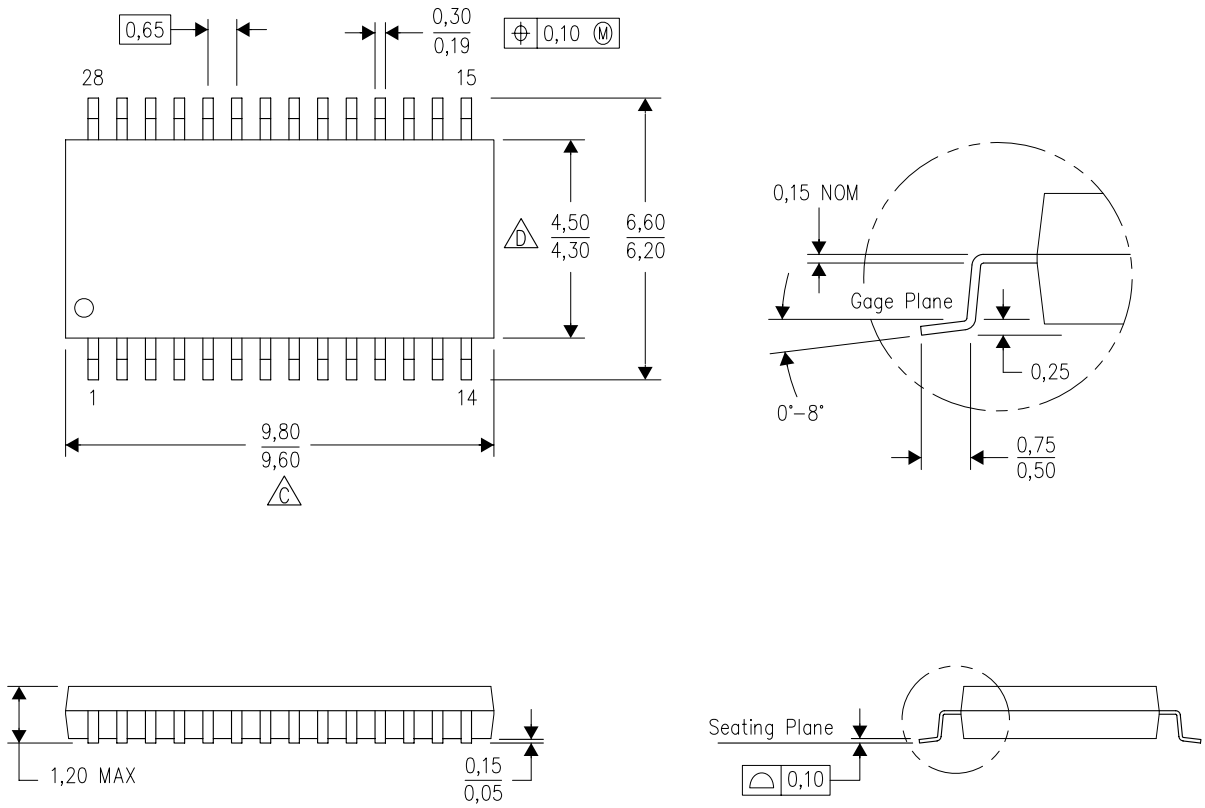
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS1030CPWR	TSSOP	PW	28	2000	367.0	367.0	38.0
THS1030IPWR	TSSOP	PW	28	2000	367.0	367.0	38.0

DW (R–PDSO–G28) PLASTIC SMALL OUTLINE



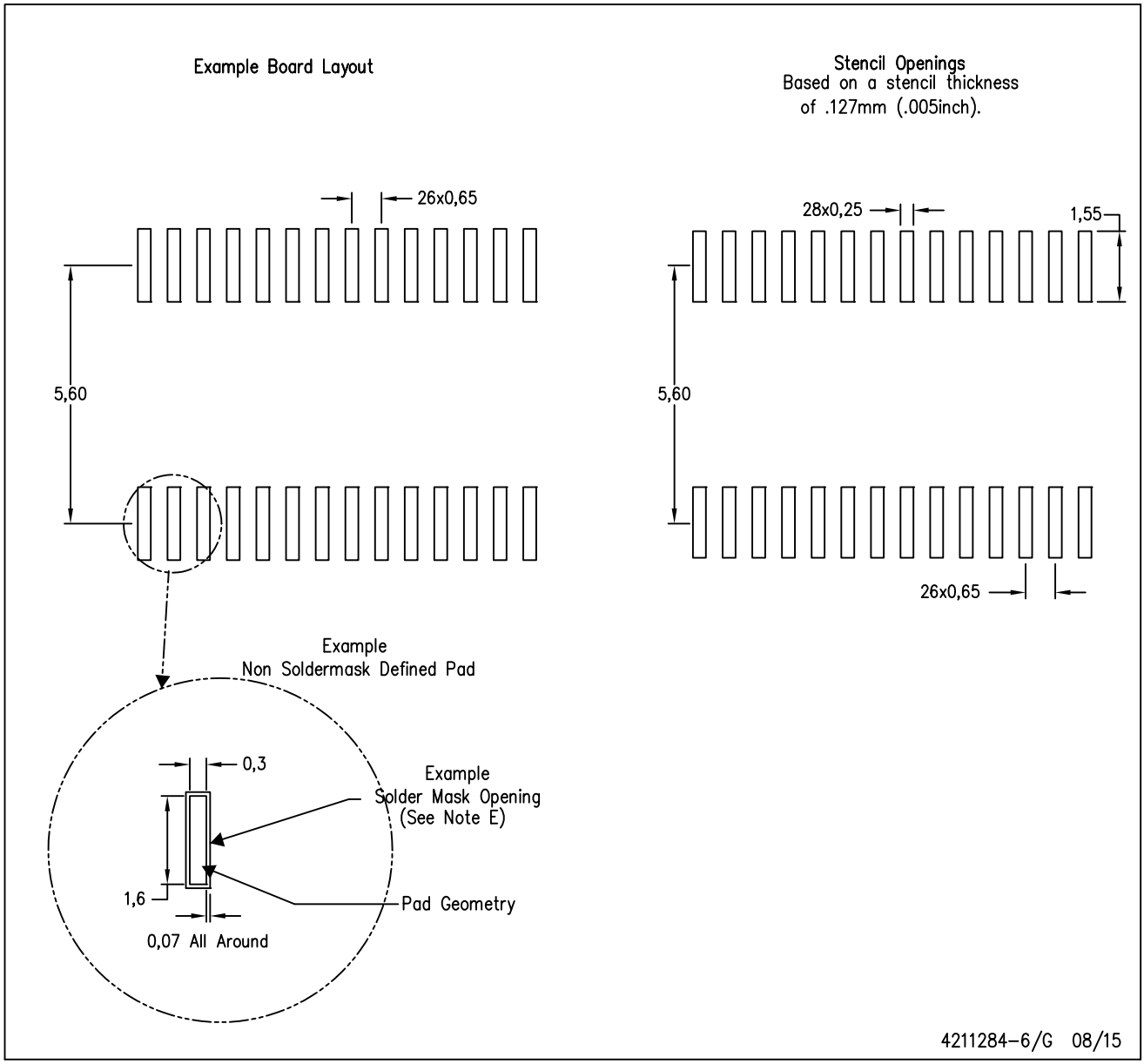
NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AE.

PW (R-PDSO-G28) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO-153

PW (R–PDSO–G28) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
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